IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Original): A phase change memory device comprising:

a semiconductor substrate;

a plurality of cell arrays stacked above said semiconductor substrate, each cell array having memory cells arranged in a matrix manner for storing resistance values as data that are determined by phase change of said memory cells, bit lines each commonly connecting one ends of plural memory cells arranged in a first direction of said matrix and word lines each commonly connecting the other ends of plural memory cells arranged in a second direction of said matrix;

a read/write circuit formed on said semiconductor substrate as underlying said cell arrays for reading and writing data of said cell arrays;

first and second vertical wirings disposed outside of first and second boundaries that define a cell layout region of said cell arrays in said first direction to connect said bit lines of the respective cell arrays to said read/write circuit; and

third vertical wirings disposed outside of one of third and fourth boundaries that define said cell layout region in said second direction to connect said word lines of the respective cell arrays to said read/write circuit.

Claim 2 (Original): The phase change memory device according to claim 1, wherein each said memory cell has a stack structure of a chalcogenide and a diode as disposed at each cross portion of said bit lines and word lines in the respective cell arrays.

Claim 3 (Original): The phase change memory device according to claim 2, wherein

said diode of said memory cell is serially connected to said chalcogenide while having a polarity with said bit line side as a cathode and with said word line side as an anode, and wherein

said bit lines and word lines are so potentially fixed as to reversely bias said diode in a non-selected mode, while a selected bit line and a selected word line are pulse driven in negative and positive directions, respectively, in data read and write modes.

Claim 4 (Original): The phase change memory device according to claim 1, wherein

said cell arrays are so stacked as to share bit lines and word lines with adjacent two cell arrays.

Claim 5 (Original): The phase change memory device according to claim 1, wherein

said first to third vertical wirings are contact plugs which are buried in an interlayer dielectric film surrounding said cell arrays.

Claim 6 (Original): The phase change memory device according to claim 1, wherein

neighboring two memory cells in each said cell array constitute a pair cell for storing complementary data one of which is a high resistance value state, and the other is a low resistance value state, and wherein

said complementary data of said pair cell are read out to a bit line pair as one bit of data.

Claim 7 (Original): The phase change memory device according to claim 6, wherein

said pair cell is selected such that another bit line is disposed between said bit line pair to which said complementary data are read out.

Claim 8 (Original): The phase change memory device according to claim 1, wherein said read/write circuit comprises:

a global bus region having a plurality of data lines to which read data are transferred and a plurality of write pulse signal lines for transferring write pulses to said bit lines, said data lines and said write pulse signal lines being so disposed as to cross a central portion of said cell layout region in said second direction;

first and second bit line select circuits disposed along said first and second boundaries of said cell layout region, respectively, to which the respective bit lines of neighboring two cell arrays are connected;

first and second sense amp arrays for sensing data of bit lines selected by said first and second bit line select circuits, respectively, said first and second sense amp arrays being disposed between said first, second bit line select circuits and said global bus region, respectively;

a word line select circuit disposed along one of said third and fourth boundaries of said cell layout region, to which shared word lines of said neighboring two cell arrays are connected; and

a write circuit disposed along the other of said third and fourth boundaries of said cell layout region for generating said write pulses supplied to said write pulse signal lines.

Claim 9 (Currently Amended): The phase change memory device according to claim 8, wherein

said shared word lines are simultaneously activated for a certain range which is selected by said word line select circuit, and the respective bit lines of said neighboring two

cell arrays are simultaneously selected for the respective certain ranges which are selected by said first and second bit line select circuits, respectively, ~~thereby simultaneously accessing to~~ so that the respective plural memory cells in said neighboring two cell arrays are simultaneously accessed.

Claim 10 (Original): The phase change memory device according to claim 9, wherein said first and second sense amp arrays have sense amps for simultaneously sensing data of the respective plural memory cells which are simultaneously selected in said neighboring two cell arrays, sensed data of which are simultaneously transferred to said data lines in said global bus region.

Claim 11 (Original): The phase change memory device according to claim 9, wherein said write circuit is configured to simultaneously output write pulses, which are to be transferred to the respective plural bit lines simultaneously selected in said neighboring two cell arrays, to said write pulse signal lines in said global bus region.

Claim 12 (Original): The phase change memory device according to claim 8, wherein neighboring two memory cells in each said cell array constitute a pair cell for storing complementary data, one of which is a high resistance value state and the other is a low resistance value state, and wherein

each of said first and second sense amp arrays comprises differential type current sensing amplifiers arranged therein, each of said current sensing amplifiers being connected to a bit line pair to which said pair cell is connected for sensing a current difference due to said complementary data.

Claim 13 (Original): The phase change memory device according to claim 8, wherein said write circuit comprises:

a logic pulse generation circuit for generating positive logic pulses and negative logic pulses to be supplied to selected word lines and selected bit lines in each said cell array, respectively, said positive logic pulses and negative logic pulses being controlled to have overlap widths therebetween in correspondence with write data; and

a write pulse generation circuit for selectively boosting said negative logic pulses output from said logic pulse generation circuit in correspondence with write data to output said write pulse signal lines.

Claim 14 (Original): The phase change memory device according to claim 13, wherein

said logic pulse generation circuit comprises:

a pulse generation circuit for generating two pulses with the same pulse width, which are phase-shifted each other; and

a logic gate circuit for outputting said negative logic pulses and positive logic pulses with an overlap time determined by combination logics determined depending on write data.

Claim 15 (Currently Amended): The phase change memory device according to claim 1, wherein

said plurality of cell arrays comprise:

a first cell array having a plurality of mutually parallel first bit lines formed on an interlayer dielectric film covering said read/write circuit, a plurality of memory cells laid out on each first bit line at a ~~prespecified~~ certain pitch, and a plurality of first word lines laid out

on said memory cells in such a manner as to commonly connect together plural memory cells aligned in a direction crossing said first bit lines;

a second cell array being formed above said first cell array while sharing said first word lines with said first cell array and having a plurality of memory cells arrayed in the same layout as said first cell array and a plurality of second bit lines overlying the memory cells in such a manner as to commonly connect together plural memory cells aligned in a direction crossing said first word lines;

a third cell array being formed above said second cell array while sharing said second bit lines with said second cell array and having a plurality of memory cells laid out in the same layout as said second cell array and a plurality of second word lines overlying the memory cells in such a manner as to commonly connect together plural memory cells aligned in a direction crossing said second bit lines; and

a fourth cell array being formed above said third cell array while sharing said second word lines with said third cell array and having a plurality of memory cells disposed in the same layout as the memory cells of said third cell array and a plurality of third bit lines overlying the memory cells in such a manner as to commonly connect together plural memory cells aligned in a direction crossing said second word lines.

Claim 16 (Original): The phase change memory device according to claim 15, wherein

said memory cell of each said cell array has a chalcogenide and a diode which are stacked at each corresponding cross portion of said first to third bit lines and said first and second word lines.

Claim 17 (Original): The phase change memory device according to claim 16, wherein

the lamination order of said chalcogenide and diode is inverse between upper and lower neighboring cell arrays, and said diode is formed to have a polarity with the side of said first to third bit lines as a cathode.

Claim 18 (Original): The phase change memory device according to claim 15, wherein

said read/write circuit comprises:

a global bus region having a plurality of data lines to which read data are transferred and a plurality of write pulse signal lines for transferring write pulses to said bit lines, said data lines and said write pulse signal lines being so disposed as to cross a central portion of said cell layout region in said second direction;

a first bit line select circuit disposed along said first boundary of said cell layout region, to which said first and third bit lines are commonly connected;

a second bit line select circuit disposed along said second boundary of said cell layout region, to which said second bit lines are connected;

first and second sense amp arrays for sensing data of bit lines selected by said first and second bit line select circuits, respectively, said first and second sense amp arrays being disposed between said first, second bit line select circuits and said global bus region, respectively;

a word line select circuit disposed along one of said third and fourth boundaries of said cell layout region, to which said first and second word lines are connected; and

a write circuit disposed along the other of said third and fourth boundaries of said cell layout region for generating said write pulses supplied to said write pulse signal lines.

Claim 19 (Original): The phase change memory device according to claim 18, wherein

said word line select circuit is configured to simultaneously activate a certain range of either one of said first and second word lines, and wherein

said first and second bit line select circuit are configured to simultaneously select a certain range of either one of said first and third bit lines, and simultaneously select a certain range of said second bit lines, respectively.

Claim 20 (Original): The phase change memory device according to claim 19, wherein

said first and second sense amp arrays have sense amps for simultaneously sensing data of the respective plural memory cells which are simultaneously selected in said first and second cell arrays or in said third and fourth cell arrays, sensed data of which are simultaneously transferred to said data lines in said global bus region.

Claim 21 (Original): The phase change memory device according to claim 19, wherein

said write circuit is configured to simultaneously output write pulses, which are to be transferred to the respective plural bit lines simultaneously selected in said first and second cell arrays or in said third and fourth cell arrays, to said write pulse signal lines in said global bus region.

Claim 22 (Original): The phase change memory device according to claim 15, wherein

neighboring two memory cells sharing said first or second word lines in each of said first to fourth cell arrays constitute a pair cell for storing complementary data one of which is a high resistance value state, and the other is a low resistance value state, and wherein

said complementary data of said pair cell are read out to a bit line pair as one bit of data.

Claim 23 (Original): The phase change memory device according to claim 22, wherein

said pair cell is selected such that another bit line is disposed between said bit line pair to which said complementary data are read out.